REMARKS

Claims 1-4 and 6-27 are currently pending in the subject application and are presently under consideration. A version of the claims is at pages 2-6. Independent claims 1, 13 and 17 have been amended herein to cure minor informalities in response to the discrepancy identified by the Examiner in the 35 U.S.C. §112, second paragraph rejection on Page 3 of the Final Office Action (dated April 4, 2006). Entry of these amendments is respectfully requested, as such amendments do not necessitate a new search and do not require undue effort on the part of the Examiner. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1-4 and 6-12 Under 35 U.S.C §112

Claims 1-4 and 6-12 stand rejected under 35 U.S.C §112, first paragraph, as failing to comply with the description requirement. In view of the amendments to independent claim 1 and the description in the instant specification at page 15, line 13 - page 16, line 2 and corresponding Figure 8, this rejection is now believed to be moot and should be withdrawn.

II. Rejection of Claims 1-4 and 6-23 Under 35 U.S.C §112

Claims 1-4 and 6-23 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In view of the amendments to independent claims 1, 13 and 17, this rejection should be withdrawn.

III. Rejection of Claims 1-14 and 17-26 Under 35 U.S.C. §102(e)

Claims 1-14 and 17-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Le *et al.* (US 6,690,602). This rejection should be withdrawn for at least the following reasons. Le *et al.* does not disclose all features of the subject claims.

> A single prior art reference anticipates a patent claim only if it ***expressly or inherently describes each and every limitation set forth in the patent claim***. *Trintec Industries, Inc. v. Top-U.S.A. Corp.,* 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631,

> 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The ***identical invention must be shown in as complete detail as is contained in the … claim***. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

The claimed invention relates to a core-based multi-bit memory having a dual bit dynamic referencing architecture fabricated on a memory core comprising a plurality of data cells. Independent claim 1 recites an architecture that facilitates a reference voltage in a multi-bit memory, comprising a multi-bit memory core including a plurality of data cells for storing data; first and second reference arrays of a plurality of multi-bit reference cells fabricated on the memory core, pairs of the plurality of the multi-bit reference cells each associated with separate wordlines within the multi-bit memory core; and a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array ***to arrive at the reference voltage employed during a data cell read operation***. Independent claims 13, 17 and 24 recite similar features. Le *et al.* does not disclose such novel features of the subject claims.

Le *et al.* relates to a system having a memory cell array and associated reference arrays. On page 5 of the Final Office Action, the Examiner incorrectly contends that the cited reference teaches a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array ***to arrive at the reference voltage employed during a data cell read operation.*** To the contrary, Le *et al.* averages voltage levels of core and reference cells to effectuate programming and erasing within the memory cells. On the other hand, for example, the claimed invention employs the reference voltage derived from the averaging procedure to ascertain whether a data bit from a memory cell is programmed or unprogrammed. Therefore, Le *et al.* does not employ the reference voltage during a data cell read operation; rather, the reference utilizes the average voltage to facilitate erase procedures in memory cells. Thus, Le *et al.* does not disclose that the average reference voltage is ***employed during a data cell read operation***, as afforded by the claimed invention.

Furthermore, claims 11 and 25 recite similar features, namely ***the first and second reference arrays including corresponding reference cells that are interweaved among the plurality of data cells.*** On page 7 of the Final Office Action, the Examiner incorrectly asserts that Figure 4 of Le *et al.* teaches the features recited in claims 11 and 25. At the indicated

portions, the reference teaches a core cell and two reference cells, and further discloses that data from the core cell is compared to an average value of the two reference cells during programming/erase verification procedures. However, Figure 4 of Le *et al.* does not address the placement of the reference cells amongst the core cells. The cited reference further shows a sector of core cells and two reference arrays (*See* Figure 3). While both the core cell sector and the reference arrays include multi-bit data cells, the reference does not teach that data cells of the reference arrays are interspersed amongst the core cells. Therefore, Le *et al.* does not afford the increased accuracy of the reference voltage with respect to data bit values of the data cell sectors as the claimed invention provides with ***the first and second reference arrays including corresponding reference cells that are interweaved among the plurality of data cells***.

Moreover, independent claim 13 further recites first and second reference arrays of a plurality of multi-bit reference cells ***fabricated on the memory core interstitial to the groups of data sectors***. Le *et al.* does not provide such an arrangement; instead, as noted above, while Le *et al.* shows a sector of core data cells in the same memory array as two reference arrays with corresponding reference cells, the cited reference does not show that the reference cells are interweaved amongst the core cells. Similarly, the cited reference does not disclose disposing reference cells interstitial to two core data cell sectors, as afforded by independent claim 13.

In view of at least the foregoing it is readily apparent that Le *et al.* does not teach the identical invention in as complete detail as is contained in the subject claims. Accordingly, this rejection with respect to independent claims 1, 13, 17 and 24 (and the claims that depend from) should be withdrawn.

IV. Rejection of Claims 16 and 27 Under 35 U.S.C. §103(a)

Claims 16 and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Le *et al.* in view of Kurihara *et al.* (US 6,791,880). Applicants' representative respectfully requests withdrawal of this rejection for at least the following reasons. The subject claims depend from independent claims 1 and 24. As discussed above, Le *et al.* does not teach or suggest applicants' invention as recited in such independent claims; and Kurihara *et al.* does not make-up for the aforementioned drawbacks of the primary reference. Accordingly, this rejection should be withdrawn.

V. Rejection of Claim 15 Under 35 U.S.C. §103(a)

Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Le *et al.* in view of Ferrant (US 6,538,942). This rejection should be withdrawn for at least the following reasons. The subject claim depends from independent claim 1. As noted above, Le *et al.* does not disclose or suggest all features of independent claim 1, and Ferrant does not compensate for the drawbacks of the primary reference. Therefore, withdrawal of this rejection is respectfully requested.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP975US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

AMIN, TUROCY & CALVIN, LLP

/Himanshu S. Amin/
Himanshu S. Amin
Reg. No. 40,894

AMIN, TUROCY & CALVIN, LLP
24TH Floor, National City Center
1900 E. 9TH Street
Cleveland, Ohio 44114
Telephone (216) 696-8730
Facsimile (216) 696-8731